REMARKS

This is intended as a full and complete response to the Office Action dated January 26, 2007, having a shortened statutory period for response set to expire on April 26, 2007. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-34 are pending in the application. Claims 1-35 remain pending following entry of this response. Claims 28 and 31 have been amended. New claim 35 has been added to recite aspects of the invention. Applicants submit that the amendments and new claim do not introduce new matter.

Claim Rejections - 35 U.S.C. § 103

Claims 1- 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Oonk* (U.S. Patent No. 6,862,703), in view of *Deas* (U.S. Patent No. 6,065,090). Applicants respectfully traverse these rejections.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143. The present rejection fails to establish at least the first and third criteria.

In this case, *Deas* does not teach or suggest all the claim limitations. Specifically, *Deas* fails to teach "replacing at least one of a row or column… with a redundant row or column; and replacing at least one word … with a redundant word," as recited by claim 1. *Deas* only teaches selective replacement of failed memory bits, namely the part of a row limited by a block, or the part of a column limited by a block. (*Deas*, Fig. 1). More specifically, a first option is to use the full row address and a

partial column address. In this case, memory cells located in the addressed row and in the block associated with the partial column address are replaced. A second option is to use a partial row address and a full column address. In this case, only memory cells located in the addressed column and located in the block associated with the partial row address are replaced. Both cases clearly do not involve the replacement of entire rows or entire columns, *i.e.*, row or column redundancy schemes.

In contrast, claim 1 requires a strategy in which at least a row or a column containing one or more defective storage cells *and* at least a word containing one or more defective storage cells are replaced. Thus, claim 1 requires a method which combines row/column repair *and* word repair. However, the cited references fail to suggest or motivate the combination of these two repair strategies. *Oonk* considers memory repair using row redundancy *or* column redundancy. *Deas* considers memory repair using bit redundancy *only*. There is no hint or motivation in these references to combine these two concepts. Therefore, Applicants submit claim 1 is not obvious in view of a combination of *Oonk* in view of *Deas*.

For these reasons, Applicants submit that claim 1 and its dependents are allowable and withdrawal of the rejections is respectfully requested.

Claims 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Oonk* in view of Applicants' admitted prior art. These claims all depend, directly or indirectly, from claim 1 which Applicants submit is allowable for reasons discussed above. Accordingly, Applicants submit that these claims are also allowable and withdrawal of the rejections is respectfully requested

Claims 16-21, 23-25, and 27-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Schwartz* (U.S. Patent No. 6,795,942) in view of *Deas*.

Claim 16 relates to a self-repair memory device comprising at least one redundant row or one redundant column, and further, at least one block of redundant words.

In the Office Action, it is stated on page 7, lines 10-12, that *Schwartz* teaches on column 2, line 42 through column 3, line 3, a self-repairing memory device comprising: "...at least one block of redundant word elements for replacing words containing defective storage elements without replacing the entire row." Applicants respectfully submit, however, that this is not the case. In the cited passage on column 2, line 42, through column 3, line 3, of *Schwartz*, it is clearly stated that only entire rows or entire columns are replaced. There is no replacement of defective memory cells *only* extending over a part of a row or a part of a column (*i.e.*, of a word). Thus, *Schwartz* does not disclose a block of redundant words.

In the Office Action, it is also stated on page 8, lines 11 to 13, that *Schwartz* teaches "...to replace at least one word containing one or more defective storage cells with a redundant word without replacing the entire row containing the at least one word." Again, this is not the case. In the Office Action, column 2, line 42, through column 3, line 3, it is cited for evidence. However, in this passage, it is clearly stated that only entire rows or entire columns are replaced. There is not replacement of defective memory cells only extending over a part of a row or a part of a column (*i.e.*, of word redundancy). For these reasons, Applicants respectfully submit that the analysis in the Office Action regarding claim 16 is incorrect.

To summarize, there is a distinction between the concepts of column or row redundancy schemes (*i.e.*, the replacement of defective storage cells of entire rows or columns) and a word redundancy scheme (*i.e.*, the replacement of defective storage cells of a part of a row without replacing the entire row containing the word). Applicants describe in the background (e.g., paragraph [0007] of the present application) that replacing row rows or columns is a known repair strategy and that replacing "small groups of logically neighboring cells (memory word) instead of complete rows and columns" is a known repair strategy (e.g., paragraph [0008] of the application). The cited prior art fails to reach beyond this admitted prior art, because *Oonk* and *Schwartz* only teach row or column repair and *Deas* only teaches word repair, with absolutely no suggestion of combining the two.

Accordingly, Applicants submit that claim 16 and its dependents are allowable and respectfully request withdrawal of the rejections.

Claims 30 and 34 are directed to the embodiment depicted on Fig. 3 (*i.e.*, to a memory built-in self-repair (MBISR) device) containing a plurality of memories, each memory being equipped with an individual MBISR circuit, and shared word redundancy. Neither *Oonk* nor *Schwartz* relates to an MBISR device containing a plurality of memories with individual MBISR circuits. It appears from the Office Action, that this claim element (a plurality of memories with individual MBISR circuits) may not have fully appreciated as, clearly, a plurality of individual MBISR circuits with shared word redundancy is neither disclosed nor suggested in the cited references.

In the Office Action, it is stated on page 10, lines 7 to 9, that the MBISR disclosed in *Schwartz* comprises "... n fault count registers for storing a corresponding number of faults in each column having an address stored in a column address register." Reference is made to column 2, line 42, through column 3, line 3, and column 5, lines 21 to 65, and Fig. 3 of *Schwartz*.

With regard to the plural "registers," (amended claim 28 expressively requires that a plurality of registers is provided), Applicants respectfully submit that the teaching of the reference is mischaracterized. The MBISR disclosed in *Schwartz* does not contain multiple fault count registers for storing the number of faults in test columns. More specifically, when a column is tested, the EC counter 76 counts the number of faults in this column (column 9, lines 47 to 50). This column fault number is compared in comparator 90 with a column defect threshold MEC 72. Depending on the comparison result, the column is flagged for replacement or not flagged (column 9, lines 63 to 67). However, the fault count is not stored and there are no multiple fault count registers for storing fault counts. There is only one fault count register, namely the EC counter 76, which, however, is reset at each new column test (column 9, line 3).

It is to be noted that the provisions of a plurality of n fault count registers according to claim 28 makes it possible that the columns to be replaced are identified after a single pass through all columns. In contrast thereto, in *Schwartz*, multiple

passes through all columns (with decreasing column defect thresholds) are needed in order to identify the columns to be replaced (column 10, lines 30 to 33). Thus, the provision of n fault count registers may shorten the total test time. Claim 31 has limitations similar to claim 28, except that the claim relates to row redundancy rather than column redundancy. Thus the same deficiencies of the prior art discussed above apply to this claim.

For these reasons, Applicants respectfully submit that claim 28 and its dependents are allowable and withdrawal of this rejection with respect to these claims is respectfully requested.

Claims 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Schwartz*. These claims depend from claim 21, which Applicants submit is allowable for reasons discussed above. Accordingly, Applicants submit these claims are also allowable and respectfully request withdrawal of this rejection.

Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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